A Novel Low Common-Mode Voltage Modulation Strategy for ANPC-5L Inverter

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Abstract. In order to suppress the leakage current of the active neutral point clamed five-level (ANPC-5L) inverter, this paper proposes a novel low common-mode voltage (CMV) modulation strategy based on the space vector modulation thought. Only the 55 voltage vectors with low CMV amplitude instead of all 125 voltage vectors are utilized. The CMV amplitude is suppressed to one-twelfth of the DC bus voltage (V_{dc}). In the simplified five-level space vector diagram, "obtuse triangle" synthesis principle is used to control the CMV changes twice in each carrier cycle, and get lower output current total harmonic distortion (THD). According to the vector thought, a carrier implementation method based on zero sequence voltage injection and carrier splitting is proposed. This method simplifies the calculation and is easy to implement. Simulation results prove the correctness and feasibility of this low CMV modulation strategy.

1 Introduction

With the development of power electronics technology, multilevel inverters have been gradually applied to the field of medium voltage and high power. Compared to traditional three-level inverters, ANPC-5L has a higher voltage level and lower current THD, moreover, its some output levels contain a redundant state, making the flying capacitor voltage and midpoint potential control simpler and more reliable[1]. However, because the output of the inverter contains high frequency CMV, leakage current is generated in the system, which reduces the safety and reliability of the system [2].

Suppressing the CMV amplitude and reducing its change frequency can effectively suppress the leakage current[3]. One is to improve the topology of the inverter or add a passive filter[4],[5], but they increase the size and cost of the inverter; the other is to optimize the modulation strategy, which is more economical and easier to implement. Therefore, many different modulation strategies have been proposed. Reference [6] proposed a five-level multi-objective optimization modulation strategy based on zero-sequence voltage injection, but its CMV amplitude can only be suppressed to one-fourth of V_{dc}. Reference [7] proposed a five-level low CMV modulation. It selects low CMV vector at each node, and uses the "last three vectors" synthesis principle to synthesize reference vectors and suppress the CMV amplitude to $V_{dc}/12$. However, the CMV changes 4 times within a carrier cycle, so the leakage current suppression effect is limited. Reference [1] proposed a modulation strategy with leakage current suppression capability (SLCPWM). It uses the combination of "obtuse angle synthesis principle" and "right angle synthesis principle", which suppresses the CMV amplitude to $V_{dc}/12$ and makes the CMV change 2 times within a carrier cycle. Although this strategy optimizes the leakage current suppression effect, it sacrifices the output current THD. In summary, the use of a suitable modulation strategy can economically suppress leakage current. However, there is still some room for optimization in the ANPC-5L inverter modulation strategy.

In order to suppress the leakage current and further optimize the output current THD. This paper proposes a novel low CMV modulation strategy. To suppress the CMV amplitude, the vector with the smallest CMV amplitude at each node is used to synthesize the reference vector. At the same time, the "obtuse triangle" synthesis principle is adopted in the simplified space vector diagram, which is to control the lowest change frequency of the CMV and the lower output current THD. For the purpose of simplifying the calculation, according to the unified theory of space vector modulation and carrier modulation[8],[9], the proposed strategy is realized by injecting the zero sequence component and cooperating with the carrier method of modulation wave splitting. Finally, the simulation verifies the correctness and feasibility of the proposed strategy in this paper.

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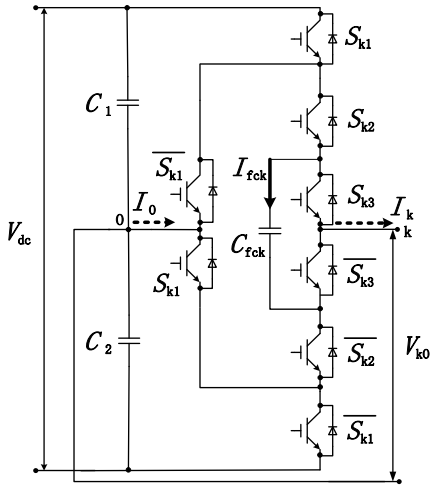


Figure 1. Phase-legs structure of ANPC-5L inverter.

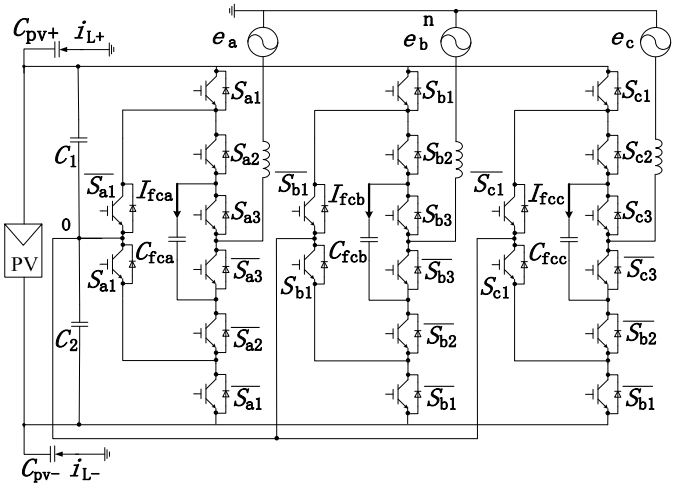


Figure 2. Three phase-legs structure of ANPC-5L inverter.

2 Principle operation of ANPC-5L inverter

The k-phase (k = a, b, c) topology of the ANPC-5L inverter is shown in Figure 1. V_{dc} is expressed as the total voltage of the DC bus, and the three-phase bridge arms are connected in parallel on the DC bus. In order to ensure the normal operation of the inverter, the voltages on the DC side upper capacitor C_1 and lower capacitor C_2 should be controlled to $V_{dc}/2$, and the flying capacitor C_{fck} voltage should be $V_{dc}/4$[1]. The positive directions of bridge arm output current I_k, flying capacitor current I_{fck} and midpoint current I_o are shown in Figure 1. Due to the same and complementary relationship in the operation of the switch tube, taking the midpoint o of the DC bus as the reference zero point, each phase bridge arm can output 5 different levels and the 8 switch states as shown in table 1. S_{k1}, S_{k2} and S_{k3} are the switch states of the switch tube, V_{ko} is the single-phase output voltage, I_{fck} and I_o are the corresponding midpoint current and flying capacitor current.

Table 1. Switch states and all currents flow relation of ANPC-5L.

S_{k1}	S_{k2}	S_{k3}	V_{ko} (V)	I_{fck} (A)	I_o (A)	switch status
1	1	1	$V_{dc}/2$	0	0	V_7
1	1	0	$V_{dc}/4$	$+I_k$	0	V_6
1	0	1	$V_{dc}/4$	$-I_k$	I_k	V_5
1	0	0	0	0	I_k	V_4
0	1	1	0	0	I_k	V_3
0	1	0	$-V_{dc}/4$	$+I_k$	I_k	V_2
0	0	1	$-V_{dc}/4$	$-I_k$	0	V_1
0	0	0	$-V_{dc}/2$	0	0	V_0

It can be seen from table 1 that the output level corresponding to the switch states of V_1 and V_2 is $-V_{dc}/4$; the output level corresponding to the switch states of V_5 and V_6 is $V_{dc}/4$. Among them, V_1 and V_5 discharge the flying capacitor voltage; V_2 and V_6 charge the flying capacitor voltage. Therefore, the flying capacitor voltage can be controlled by selecting an appropriate redundancy state.

The three-phase topology of the ANPC-5L inverter is shown in figure 2, where the positive and negative capacitances of the photovoltaic panel to ground are equivalent to Cpv+ and Cpv-. Suppose Cpv+ ≈ Cpv- = Cpv. Define the switching function S_k (k = a, b, c) as shown in equation (1).

$$S_k = \begin{cases} 2 \cdots\cdots V_7 \\ 1 \cdots\cdots V_6、V_5 \\ 0 \cdots\cdots V_4、V_3 \\ -1 \cdots\cdots V_2、V_1 \\ -2 \cdots\cdots V_0 \end{cases} \quad (1)$$

The output voltage of each phase is:

$$V_{ko} = S_k \cdot \frac{V_{dc}}{4} \quad (2)$$

Therefore, the five-level inverter can output $5^3 = 125$ voltage combinations. In the abc coordinate system, the voltage spatial reference vector V_{ref} [9] is defined as：

$$V_{ref} = \frac{V_{dc}}{4} \cdot \left(S_a + \alpha \times S_b + \alpha^2 \times S_c\right) \quad (3)$$

In the equation (3), $\alpha = e^{j\frac{2\pi}{3}}$.

According to equation (3), the five-level inverter space vector diagram as shown in figure 3, where the three numbers of each combination from left to right represent the three-phase switching functions S_a, S_b, S_c. 125 switching function combinations represent 125 space vectors[1].

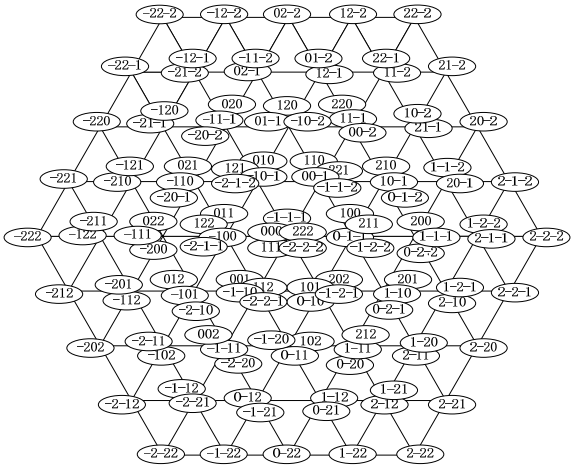


Figure 3. Voltage space vector diagram of ANPC-5L.

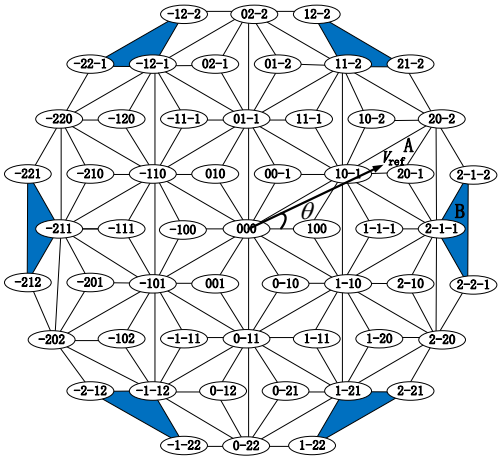


Figure 4. Simplified space vector diagram of ANPC-5L.

3 Proposed Low CMV modulation strategy based on vector thought

The expressions of leakage current i_L and CMV V_{cm} are shown in equations (4),(5)[1]:

$$i_L = 2C_{pv}\frac{dV_{cm}}{dt} \tag{4}$$

$$V_{cm} = \frac{V_{dc}}{12}\cdot\left(S_a + S_b + S_c\right) \tag{5}$$

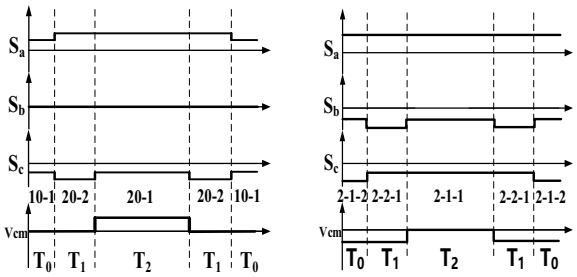
It can be seen from equation (4) that by suppressing the V_{cm} and dV_{cm}/dt, the leakage current can be effectively suppressed.

3.1 Suppress V_{cm} amplitude

It can be known from equation (5) that reducing the sum of three-phase switching functions S_a, S_b and S_c can effectively suppress the CMV amplitude. Therefore, the proposed scheme uses 55 vectors instead of the 125 vectors in figure 3, which make the CMV vary from -$V_{dc}/12$ to $V_{dc}/12$. The simplified space vector diagram is shown in figure 4, which reserves the minimum sum of S_a, S_b and S_c on each node, and discards the vectors on the 6 nodes of the outermost hexagon, that is, (2,-2,-2), (2,2,-2), (-2,2,-2), (-2,2,2), (-2,-2,2), (2,-2,2). In addition the inverter can still operate up to the maximum modulation index[7].

3.2 Reduce the frequency of V_{cm} change

In order to further suppress the leakage current, at the same time take into account the effect of different modulation strategies on the output current THD. This paper proposes a novel low CMV modulation strategy, which uses the synthesis principle of "obtuse angle three vectors" in the simplified space vector diagram. Taking the area A and B as examples, when the reference vector V_{ref} is located in area A, the V_{ref} is synthesized using (1, 0, 1), (2, 0, 2), (2, 0, 1); when the reference vector V_{ref} is located in area B, V_{ref} is synthesized using (2, 1, 2), (2, 2, 1), (2, 1, 1). The switch sequence and CMV in area A and B are shown in figure 5. The proposed strategy realizes that CMV changes twice in a carrier cycle.



(a) V_{ref} is in area A. (b) V_{ref} is in area B.

Figure 5. Switch sequence and CMV in area A and B.

In summary, compared with the combination method of "obtuse angle synthesis principle" and "right angle synthesis principle" adopted in reference [1], the proposed strategy is closer to the "recent three-vector" synthesis principle, therefore it has better output current THD characteristics.

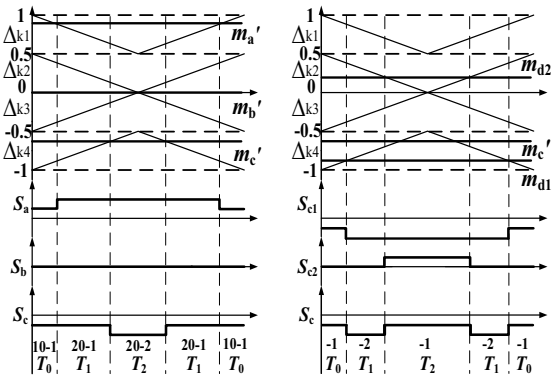
4 Implementation method of the proposed strategy carrier

In order to simplify the complex area division of space vector modulation and the calculation of synthetic vector action time. In this paper, a method based on carrier stacking is used to achieve the proposed strategy by means of injection of zero-sequence voltage (m_0) and modulation wave splitting.

4.1 Carrier implementation method

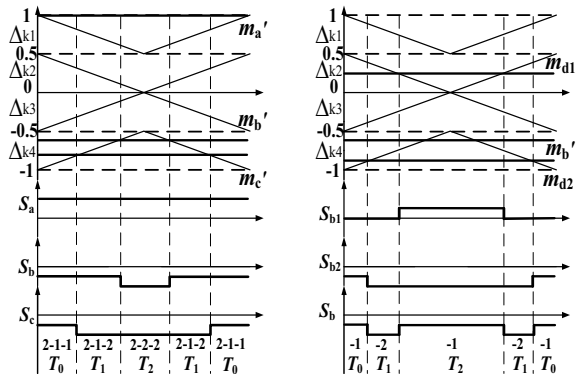
4.1.1. Discuss the situation when V_{ref} is in area A. It can be seen from figure 5(a):

① Phase B is clamped to 0; ② Phases A and C change at the beginning and end of T_1 at the same time; ③ Phase C sequence double frequency action.



(a) Inject m_0. (b) Split C-phase.

Figure 6. Modulate and carrier wave in area A.



(a) Inject m_0. (b) Split B-phase.

Figure 7. Modulate and carrier wave in area B.

Firstly, inject the m_0 to satisfy the condition ①, specifically expressed as:

$$m_0 = -m_b \tag{6}$$

The modulated waves m_a' , m_b' , m_c' and the carrier after injecting m_0 are shown in figure 6(a), comparing figure 5(a), the double-frequency switching sequence of phase C cannot be obtained only by clamping phase B. A modulation wave splitting method is used here. Firstly, m_c' is split into two modulation waves, m_{d1} and m_{d2}, which are compared with the carrier to obtain S_{c1} and S_{c2}, then the S_c of phase C is the sum of S_{c1} and S_{c2}, as shown in figure 6(b). To keep the duty cycle of phase C unchanged and satisfy the condition ②, ③, phase C splits into:

$$\begin{cases} m_{d1} = -m_a^{'} \\ m_{d2} = m_c^{'} - m_{d1} \end{cases} \tag{7}$$

4.1.2. Discuss the situation when V_{ref} is in area B. It can be seen from figure 5(b):

① Phase A is clamped to 2; ② Phases B and C change at the beginning and end of T_1 at the same time; ③ Phase B sequence double frequency action.

Firstly, inject the m_0 to satisfy the condition ①, specifically expressed as:

$$m_0 = 1 - m_a \tag{8}$$

The carrier wave and modulated wave are shown in figure 7(a). As in the area A, m_b' is split into two modulation waves, m_{d1} and m_{d2}, and the split B-phase modulation wave is shown in figure 7(b). According to conditions ②, ③ , m_{d1} and m_{d2} can be obtained:

$$\begin{cases} m_{d1} = -m_c^{'} - 0.5 \\ m_{d2} = m_b^{'} - m_{d1} \end{cases} \tag{9}$$

The analysis method of other sectors is the same as the sectors shown by $0 \le \theta \le \pi/6$, and will not be described here.

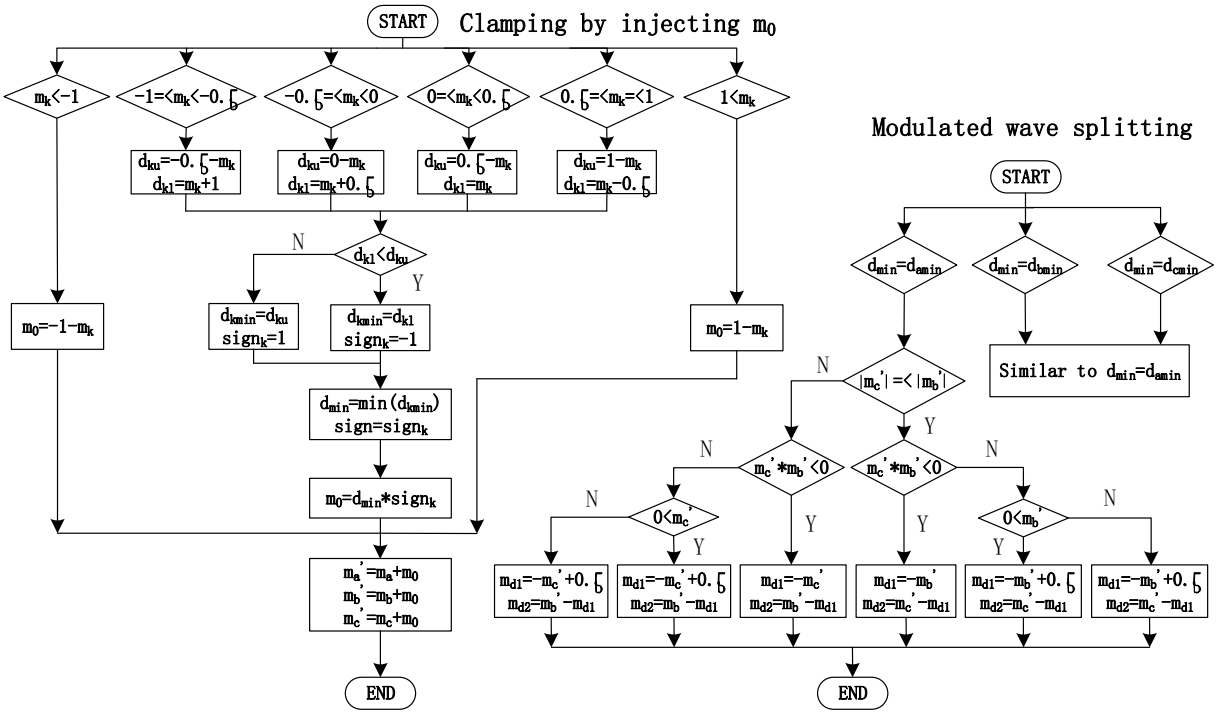


Figure 8. The steps for obtaining m_0 and the modulated wave splitting.

4.2 Carrier implementation steps

Summarize the carrier realization method of 4.1 regularly, the specific steps of carrier realization are as follows.

4.2.1. Clamping by injecting m_0 and modulated wave splitting. The steps for obtaining m_0 and the modulated wave splitting are shown in figure 8. The variable d_{ku} (d_{kl}) is the distance between m_k and the upper (lower) boundary in the divided range in figure 8. Finally get the modulated waves m_a' , m_b' , m_c' and one phase split modulation waves m_{d1} , m_{d2}. Take phase C split as an example, compare m_a' and m_b' with the reverse stacked carrier to get the phase A and B switching sequences S_a and S_b; then compare m_{d1} and m_{d2} with the reverse stacked carrier to get the switching sequences S_{c1}, S_{c2}, finally the sum of S_{c1} and S_{c2} generates the c-phase switching sequence S_c.

4.2.2. Control of flying capacitor voltages. Use the redundant switch states V_5, V_6 and V_1, V_2 corresponding to the output levels $V_{dc}/4$ and $-V_{dc}/4$ in table 1 to balance the flying capacitor voltage. Depending on V_5, V_6 , V_1, V_2 and the phase current direction, the flying capacitor can be charged or discharged.

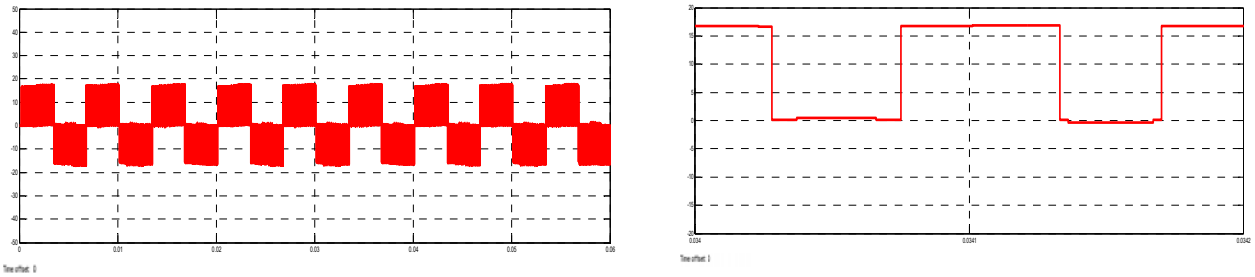
5 Simulation results

In order to verify the effectiveness of the modulation strategy proposed in this paper, a simulation model was built in Matlab/Simulik. The simulation parameters are shown in table 2.

Table 2. Simulation parameters.

Parameters	Values
Total DC bus voltage	200V
Upper and lower bus capacitors	3mF
Flying capacitors	470μF
Carrier frequency	10kHz
Load resistance	10Ω
Load inductance	1.5mH
Modulation degree	1
Output frequency	50H

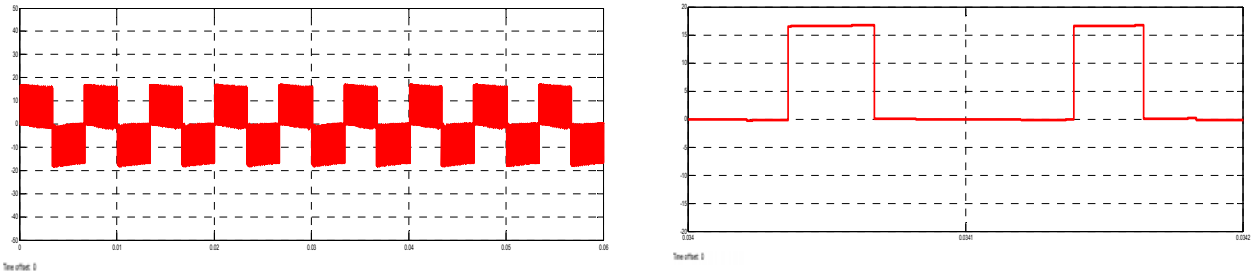
Figure 9(a) is the CMV waveform under the SLCPWM modulation strategy, we can see that the amplitude of the CMV is 16.6V, which is $V_{dc}/12$; figure 9(b) is a partial enlarged view of the CMV, it can be seen that the number of CMV change is 2 times in a carrier cycle.



(a) Overall view. (b) Partially enlarged view.

Figure 9. The CMV waveform under SLCPWM modulation strategy.

Figure 10(a) is the CMV waveform under the modulation strategy proposed in this paper. The CMV amplitude is also $V_{dc}/12$, and the number of CMV change is still 2 times in one carrier cycle in figure 10(b), so the two modulation strategies have the same CMV performance.



(a) Overall view. (b) Partially enlarged view.

Figure 10. The CMV waveform under the modulation strategy proposed in this paper.

However, the THD performance under different modulation degrees is shown in table 3. It can be seen that when the modulation degree is less than 1, the modulation strategy proposed in this paper has obvious advantages in THD. With the further increase of the modulation degree, the THD gap of the two modulation strategies has narrowed. When the modulation degree is equal to 1.1, it is basically the same. In practical applications, the modulation degree will generally leave a certain margin. Therefore, the modulation strategy proposed in this paper has a certain advantage in terms of THD in general.

Table. 3 Current THD of four modulation under different modulation indices.

Modulation strategy	M=0.8	M=0.9	M=1	M=1.05	M=1.1
SLCPWM	3.25%	3.04%	2.56%	1.83%	1.45%
This paper	2.33%	1.54%	1.65%	1.82%	1.47%

6 Conclusion

Aiming at the problem of five-level leakage current, this paper proposes a low CMV modulation strategy with leakage current suppression capability, and expounds its basic principles and vector synthesis principles. This modulation strategy can suppress the CMV amplitude to be $V_{dc}/12$ in the full linear operating range, and change twice with a lower output current THD in one cycle.

In order to simplify the control method, a carrier realization method of injecting zero sequence components and modulation wave splitting is proposed, which not only simplifies the calculation amount, but also is easy to implement in engineering. Finally, the correctness and effectiveness of the proposed modulation strategy are verified by simulation.

Acknowledgments

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