# Influence of the parameters to transition capacitance at NCDS-PSI heterostructure

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**Abstract.** It is important to research the dependence of the capacitance and capacitance on the parameters on the photodiodes. In this article, we aim research experimental and theoretical on the nCdSpSi heterostructure. A heavily doped n+CdS layer with a thickness of about 50 Å was created by deposition of a thin layer of indium (In) for 25-30 s on the surface of a CdS film in vacuum with a residual pressure of 10-5Torr at a substrate temperature of 373 K, followed by annealing at 673 K in within 300s. Then, on the surface of this heavily doped n+CdS layer, a current-collecting "P"-shaped ohmic contact with an area of 3 mm2 was obtained also by the vacuum evaporation of In.

## 1 Introduction

In recent years, many photodiodes with semiconductor pn and pin transitions have been studied in scientific studies. In mass production conditions, the production of photodiode with repeatable and stable parameters are important with reducing the cost of testing and calibrating photodiode, and at the same time significantly decreasing production costs.

Photodiodes are used in consumer electronics devices such as compact disc players, smoke detectors, medical devices [1]. Transition Capacitance measurement methods for low and high frequencies are given[2].The structures were obtained by the method- by thermal spraying of powders of th binary compound CdS (semiconductor purity). CdS was deposited slowly, as described in a quasi-closed vacuum system with a residual pressure of 10-5torr [3].

Silicon wafers with a thickness of 300-350 μm, incised in the (001) and (111) crystal directions from single-crystal silicon ingots of n-and p-type conductivity with specific resistances $\rho \approx (5 - 10)$ Ω•cm, were used as substrates. The Si substrates used in the experiments were prepared in advance at the factory according to GOST, i.e., the substrates

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were obtained ready for epitaxy. However, all the same, the contaminants present on the surface of the silicon wafer, formed as a result of long-term storage, require their removal from the surface of the substrate and its refreshment. Why we used an alkaline etchant based on potassium hydroxide [4], since the substrates were completely prepared for use, which did not require the use of other cleaning methods. The etchant consisted of a 5% aqueous solution of potassium hydroxide. Etching was carried out for 8–10 minutes. After that, a thorough washing was carried out, since potassium hydroxide is poorly removed from the surface wetted with it. Washing was carried out by the displacement method [7] in two stages: first, the substrates were washed with running distilled water for 8–10 minutes, then with deionized water for 3–5 minutes. After that, the substrates were dried in an oven with infrared drying for 15–20 minutes. The reproducibility of samples of injection photodiodes obtained on substrates cleaned by the above method in 70–80% of cases was obtained with similar parameters (photosensitivity and gain), in the remaining 20–30% cases, the deviation of the main parameters was 50–80%, and in some cases it reached up to 100 - 120%.During film deposition, the temperature of the crucible with the source (CdS) was varied in the range TIST ≈ 800–850°C, while the substrate temperature (pSi) was maintained within the range TP ≈ 250–270°C. In this case, to ensure the reproducibility of the IFD structures, a shutter was used, with the help of which the CdS deposition time was set, which ensured that the film thickness was the same from experiment to experiment. Studies of the surface of samples of the obtained CdS films using an MII-4 microscope showed that CdS films consist of densely packed columnar crystallites (grains) (Fig.1), oriented in the direction of film growth and misoriented in azimuth. Even when studying the surface of the films, analyzing the state of its relief, phase contrast, potential and its structural changes caused during the technological process and under external influences, the method of atomic force microscopy (AFM) was used. By morphological studies of the films obtained by us, it was found that the sizes of crystallites strongly depend on technological modes, primarily on the substrate temperature TS. For example, CdS films produced at TS = 300°C. had crystallite sizes ~ 3÷4 μm, completely penetrating the film with thickness w ≈ 2 μm, which had n-type conductivity with resistivity ρ ≥ (2-3)106 Ω •cm.

In the preparation of samples of IFD structures, the contacts to the structures were obtained by deposition of indium (In) in a vacuum, solid from the back side onto the Si substrate. A heavily doped n+CdS layer with a thickness of about 50 Å was created by deposition of a thin layer of indium (In) for 25-30 s on the surface of a CdS film in vacuum with a residual pressure of 10-5Torr at a substrate temperature of 373 K, followed by annealing at 673 K in within 300s. Then, on the surface of this heavily doped n+CdS layer, a current-collecting "P"-shaped ohmic contact with an area of 3 mm2 was obtained also by the vacuum evaporation of In.It is known that the parameters of the crystal lattice of CdS hexagonal modification (αCdS = 5.84 Å) differ from the crystal lattice of Si (αSi = 5.43 Å) by almost 7%. However, it is clear from specialized literature that in order to create a heterojunction with a low density of surface states, their difference should not exceed 4% [8].

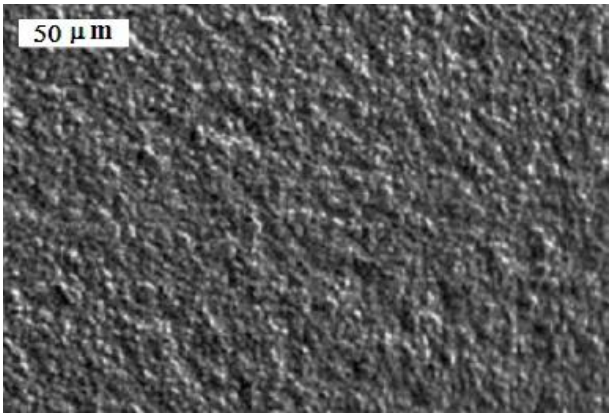


**Fig. 1.** Micrograph of the surface of an epitaxial CdS film.

However, numerous studies of surface states at the interface between the nCdS layer and the nSi substrate showed that their density turned out to be lower than expected at the beginning of the experiment. Therefore, we assume that during the formation of n+CdS-nCdS–nSi and n+CdS–nCdS–pSi hetero structures, an intermediate transition layer is formed between the CdS layer and the Si substrate, which contributes to smoothing out the difference between their crystal lattices.

In order to prove the above assumption, the distribution of chemical elements in the n+CdS – nCdS – nSi and n+CdS – nCdS – pSi hetero structures over the thickness of the CdS film was studied, which was carried out along the cleavage of the hetero structure. In the specialized literature, there are works devoted to methods for determining the geometric parameters of the created structures in a non-destructive way. For example, in [9] shows the possibility of using the X-ray spectral microanalysis (XSMA) method to determine the composition and depth of the nanoscale layer, as well as the advantages of this method. It is shown that the methods used in this work make it possible to nondestructively determine the depth, elemental composition, and geometric parameters of the ZnCdSenanolayer, which is part of the structure they obtained. Therefore, we measured the parameters and composition of the CdS layers we obtained were carried out on a Jeol-JXA-8900 microanalytical complex using an EDS (Energy Dispersive Spectrometer) LINK ISIS (Japan). Measurement conditions: U = 20 kV, I = 10 nA. The standards are native Cd and Si, and for S, synthetic FeS. The measurement error in this case was ±2.0%. The measurement results are shown in Figure 2.2.The measurement results, as well as the analysis of the micrograph, showed that the elements Cd, S, and Si at the interface sharply decrease, reaching almost zero at a distance of ~ 0.6 – 1.0 μm (from the substrate) along the film thickness (in the region marked with a dotted line in Fig. 2).Hence it follows that between the nCdS layer and the nSi substrate there is a layer of a solid solution with a thickness of 0.6 ~1.0 μm, consisting of a mixture of chemical elements that make up the pSinCdSn + CdS hetero structure. To construct the calculated C(U) characteristic, we needed the value of the concentration of equilibrium holes (p0).

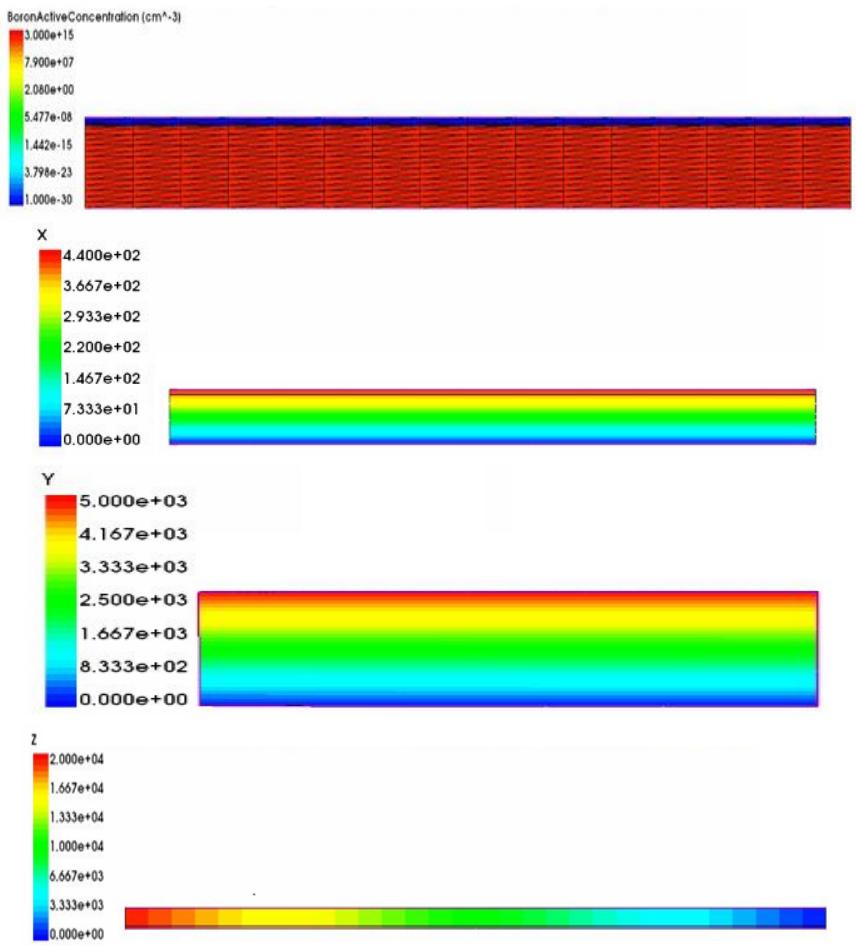


**Fig. 2.** Distribution of chemical elements over the thickness of the nCdS layer deposited on the pSi substrate.

## 2 Theoretical and experimental analysis

The analysis of the C(U)-characteristics (see Fig. 2.3) of the pSi - nCdS - n + CdS hetero structure fully confirms this. Capacitance–voltage characteristics of the pSi – nCdS–n+CdS hetero structure. One of the non-destructive methods for obtaining information about the interface is the method of the frequency capacitance-voltage characteristic (CV). The results of measurements of the C–V characteristics of the investigated nSi – nCdS – n+CdS and pSi – nCdS – n+CdS hetero structures showed that they belong to the class of MIS structures. This is logical, since the nCdS layer in these heterostructures is a highly compensated high-resistance material, and the oxide layers formed between the nCdS layer and silicon during deposition of CdS on the silicon surface can very likely behave as a dielectric. The experimental CV characteristics of the pSi – nCdS – n+CdS hetero structures were measured at room temperature (300 K) in forward and reverse bias voltages in the frequency range f = (0.4÷50) kHz. Since the C(U)-characteristics at these frequencies have the same shapes, we will consider only one of them. Therefore, Figure 2.3 shows only one curve obtained at f = 10 kHz, since at this frequency the C(U)-characteristic of the MIS

structure manifests itself more clearly. This, in turn, means that the surface states in the pSi – nCdS heterojunction are slow surface states. In addition, Fig.3 also shows the calculated (curve 2) C(U)-characteristic. The calculated C(U)-characteristic was constructed by the method, as shown in [5].

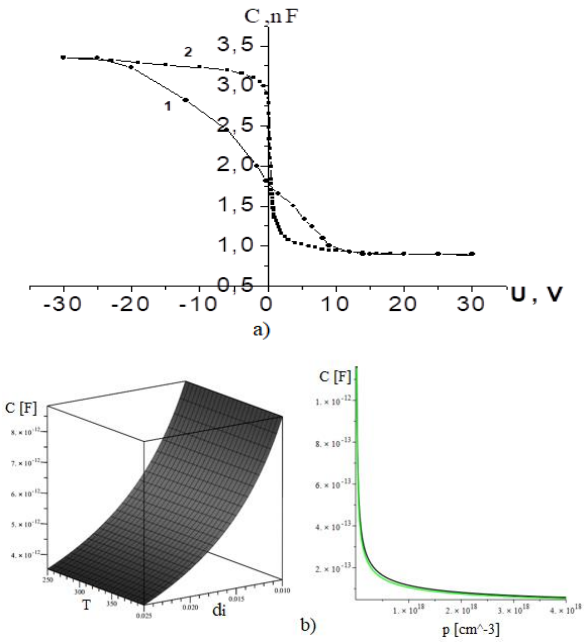


**Fig. 3.** a) C(U)-characteristic of pSinCdSn+CdS hetero structures, b) C(p) and C(p,T) characteristic of pSinCdSn+CdS hetero structures.

The concentration of equilibrium holes (p0) was determined from the capacitance of flat bands and from the steep section of the C(U) characteristic using formula (2.1). The obtained values of p0 (which turned out to be 8.3•1014 cm-3 and 2.1•1015 cm-3, respectively) indicate their inhomogeneity over the surface and thickness of the silicon. Further, according to the capacitance of the dielectric layer Ci = 3.35 nF, its thickness (di) was determined using the flat capacitor formula C = εoεS/d (where S is the area of the structure), which turned out to be equal to di ≈ 0.26 μm at the values: εo = 8.85 •10-14 F/cm, ε =10 and S ≈ 0.1 cm2. The calculated thickness of the dielectric differs from the thickness (w) of the high-resistance base (nCdS), which is equal to w ≈ 2 μm. This difference is due to the formation of oxide films of the CdOx, SOx type on the surface of the nCdS film and the oxide layer of SiOx on the surface of the pSi substrate during the deposition of the nCdS layer. Further, from the minimum capacitance of the structure Cmin ≈ 0.9 nF, the space charge thickness d ≈ 0.98 μm was determined, which is equal to almost half the base thickness (w ≈ 2 μm). And at thermodynamic equilibrium, its thickness turned out to be equal to d ≈ 0.49 μm, which was calculated from the capacitance C = 1.8 nF in the absence of bias voltage.These results are logical if we take into account that the thickness of the space charge narrows in the forward direction of the current, and in the reverse direction, on the contrary, expands with increasing bias voltage. It follows from these experimental data that the space charge resistance is the determining factor in the total resistance of the entire structure, as evidenced by the coincidence of its capacitance with the dielectric capacitance in the C(U) characteristic. As for the appearance of a plateau on the C(U)-characteristic when reverse voltage U = 25-30 V is applied (see Fig.4), this is due to

the fact that the process of space charge expansion is compensated with the process of electron injection from nCdS - pSi heterojunction.

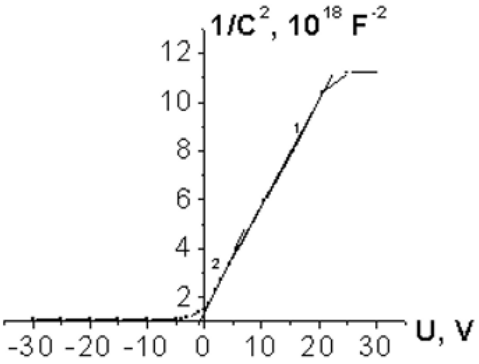


**Fig. 4.** Capacitance–voltage characteristic of the n+CdS–nCdS–pSi hetero structure in coordinates C-2(U) at a frequency f = 10 kHz and T = 300 K.

The concentration of equilibrium holes (p0) was determined from the capacitance of flat bands and from the steep section of the C(U) characteristic. To determine p0 from the C(U)-characteristic, a steep section was built in the C-2(U) coordinates, which has two slopes. From the slopes of these straight lines, the concentration of equilibrium holes p0 was determined using the well-known formula:

$$p_0 = \frac{2}{q\varepsilon_0\varepsilon_S S^2}\frac{dV_D}{d(C^{-2})}, \quad (1)$$

where q is the electron charge, ε0is the vacuum dielectric constant, εSis the permittivity of the semiconductor, VD is the potential barrier height, S is the area of the structure. Thus, the concentrations of equilibrium holes were determined to be 3.2·1015 cm-3 and 4·1014 cm-3. By extrapolating the C-2(U) dependence to the voltage axis U (see Fig.4), the potential barrier height VD = (0.89 ± 0.02) eV for p0 in pSi was determined. In addition, the value of the concentration of equilibrium holes was also estimated from the capacitance of flat bands using the formula:

$$C_{n3} = \frac{\varepsilon_0\varepsilon_i S}{d_i + \frac{\varepsilon_i}{\varepsilon_S}\sqrt{\frac{kT\varepsilon_0\varepsilon_i}{p_0 q^2}}} \quad (2)$$

where εi is the permittivity of the dielectric layer, di is the thickness of the dielectric layer, and in this case the value p0≈ 1.8·1015cm-3 is obtained. The values of p0 determined from the CV characteristics are in good agreement with the value of the equilibrium hole concentration of ≈1.3·1015 cm-3 for pSi.

## 3 Conclusion

For samples with different levels of doping of the base region, the temperature and depletion region dependence of the space charge region width of the capacitance nCdS-pSi hetero structure is studied (Fig.3). The results of the experiment were compared with the theoretically calculated results. We see that the dependence of the capacitance on the thickness of the base changes from low temperature to high temperature from linear to expansive possible. This difference is due to the formation of oxide films of the CdOx, SOx

type on the surface of the nCdS film and the oxide layer of SiOx on the surface of the pSi substrate during the deposition of the nCdS layer. Further, from the minimum capacitance of the structure Cmin ≈ 0.9 nF, the space charge thickness d ≈ 0.98 μm was determined, which is equal to almost half the base thickness (w ≈ 2 μm). And at thermodynamic equilibrium, its thickness turned out to be equal to d ≈ 0.49 μm, which was calculated from the capacitance C = 1.8 nF in the absence of bias voltage. These results are logical if we take into account that the thickness of the space charge narrows in the forward direction of the current, and in the reverse direction, on the contrary, expands with increasing bias voltage.

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